

CLAIMS

1 1. A printer comprising:
2 at least one laser driver;
3 a print control engine; and
4 a video controller, bidirectionally connected to the print control engine and the at
5 least one laser driver via a system bus, having a video block that includes,
6 a direct memory access (DMA) controller,
7 a video processor,
8 a first data bus and control bus electrically connecting the DMA controller
9 to the video processor,
10 a video signal generator, connected to the video processor,
11 a second data bus and control bus connecting the video processor to the
12 video signal generator,
13 a frequency synthesizer connected to the video signal generator,
14 configuration registers bidirectionally connected to the DMA controller,
15 video processor, the video signal generator and the frequency synthesizer, and
16 a data bus and control bus electrically connecting the DMA controller and
17 the configuration registers to the system bus.

1 2. A printer, as defined in claim 1, the data bus and control bus including:
2 a third data bus and control bus electrically connecting the configuration registers
3 to the system bus; and
4 a fourth data bus and control bus, electrically connecting the DMA controller to
5 the system bus.

1 3. A printer, as defined in claim 1, wherein the video controller generates one
2 pass of the one laser driver, the image generated being monochromatic.

1 4. A printer, as defined in claim 1, wherein the video controller generates
2 multiple passes of the laser driver, the image generated containing four color planes.

1 5. A printer, as defined in claim 1, further comprising three color laser drivers,
2 each connected to the video controller which has four video blocks, the image generated
3 being an *in-line* color image.

1 6. A printer, as defined in claim 1, wherein:
2 the video controller further includes a second video block; and
3 a second laser driver connected to the video controller.

1 7. A printer, as defined in claim 6, wherein the video controller controls sharing
2 the pass of the two laser drivers, the image generated being monochromatic.

1 8. A printer, as defined in claim 6, wherein the video controller generates
2 multiple passes for each laser driver, the image generated containing four color planes.

1 9. A printer, as defined in claim 6, further comprising seven laser drivers, each
2 connected to the video controller which has eight video blocks, the image generated
3 being in-line color image.

1 10. A scanning control circuit comprising:
2 a direct memory access (DMA) controller;
3 a video processor;
4 a first data bus and control bus electrically connecting the DMA controller to the
5 video processor;
6 a video signal generator, connected to the video processor;
7 a second data bus and control bus connecting the video processor to the video
8 signal generator;
9 a frequency synthesizer connected to the video signal generator;
10 configuration registers bidirectionally connected to the DMA controller, video
11 processor, the video signal generator and the frequency synthesizer; and
12 a data bus and control bus electrically connecting the DMA controller and the
13 configuration registers to a system bus.

1 11. A scanning control circuit, as defined in claim 10, the data bus and control
2 bus including:
3 a third data bus and control bus electrically connecting the configuration registers
4 to the system bus; and
5 a fourth data bus and control bus, electrically connecting the DMA controller to
6 the system bus.

1 12. A method for scanning a memory comprising:
2 determining a vertical direction for scanning the memory;
3 determining a horizontal direction for scanning the memory;
4 initializing the DMA address;
5 reading the data line;
6 updating the DMA address; and
7 repeating the steps of reading and updating.

1 13. A method, as defined in claim 12, wherein initializing comprises:
2 when the memory scan is top-to-bottom and left-to-right, the DMA Address is
3 initialized to the Start Address;
4 when the memory scan is top-to-bottom and right-to-left, the DMA Address is
5 initialized to the Start Address + data_per_line - 1;
6 when the memory scan is bottom-to-top and left-to-right, the DMA Address is
7 initialized to the Start Address - data_per_line * (linecount - 1); and
8 when the memory scan is bottom-to-top and right-to-left, the DMA Address is
9 initialized to the Start Address + (data_per_line * linecount) - 1.

1 14. A method, as defined in claim 12, wherein updating comprises:
2 when the memory scan is top-to-bottom and left-to-right, the DMA Address is
3 incremented to the DMA Address + (skips * data_per_line);
4 when the memory scan is top-to-bottom and right-to-left, the DMA Address is
5 incremented to the DMA Address + ((2 + skips) * data_per_line);

6 when the memory scan is bottom-to-top and left-to-right, the DMA Address is
7 incremented to the DMA Address – $((2+\text{skips}) * \text{data_per_line})$; and
8 when the memory scan is bottom-to-top and right-to-left, the DMA Address is
9 incremented to the DMA Address – $(\text{skips} * \text{data_per_line})$.

1 15. A method, as defined in claim 12, wherein reading the data line includes,
2 setting a repeat counter to the number of desired repeats,
3 reading data at the DMA address,
4 horizontally updating the DMA address according to the direction of the
5 horizontal read; and
6 when there is more data to be read, setting the DMA address to the line
7 start address;
8 when there is more data to be read, repeating the steps of reading and
9 horizontally updating.

1 16. A method, as defined in claim 15, wherein horizontally updating comprises
2 incrementing the DMA address when the read is from left to right.

1 17. A method, as defined in claim 15, wherein horizontally updating comprises
2 decrementing the DMA address when the read is from right to left.
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